ECE 241 Lab 8 – Latch or Flip-Flop?!?!

**Objective**
Use VHDL to explore the differences between latches and flip-flops.

**Experiment (15 pts)**
Develop a VHDL component which models a latch and a flip-flop, as shown below, using two separate VHDL processes. (see below!) Synthesize your design and examine any warnings. Develop a testbench* which illustrates the differences in behaviors. Examine what happens if an input changes too close to the active clock edge? How does the simulator indicate an unknown value (e.g., the initial values for Q outputs)?

**Report (5pts)**
Turn in a brief, professional report that describes your design process and results. Describe, in your own words, the differences and similarities between latches and flip-flops. Elaborate on any problems you encountered. Finally, attach to your report hardcopies of your VHDL, post-synthesis simulation, and the project summary.

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**VHDL Processes**

Statements inside of a VHDL process are executed *sequentially*. A process is “activated” when (a) one or more of the signals in the *sensitivity* list changes, or (b) when the conditions on a *wait* statement are satisfied. Once activated, the statements inside of the process execute until the process is *suspended* (i.e., the end of the process is reached or a wait statement is executed).

In this class we will use a signal sensitivity list to activate the process, as shown in Tables 8-5 and 8-6 of the text. (p. 699).

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**Testbench Instructions**

You will need to follow these instructions in order to simulate both the latch and the flip-flop since, normally, the testbench waveform editor restricts when inputs can change.

1. After selecting “Create New Source” and “Testbench Waveform” the tool will bring up a window titled “Initialize Timing.” This is the window where we have been selecting “combinational.” Instead, check the box at the bottom of the window labeled “Add Asynchronous Signal Support.” Then select “next.”
2. The next window, titled “Clock Selection,” asks you to select the clock signal. Highlight the appropriate signal and select “next.”
3. The final window is titled “Clock and Signal Association.” Highlight all of the signals under “Unassigned,” then click the “add” button, then “next” and “finish.”