13.3 (a) For the following sequential network, find the next-state equation or map for each flip-flop. Using these next-state equations or maps, construct a (Moore) state table and graph for the network.
(b) What is the output sequence when the input sequence is $X = 01100$?
(c) Draw a timing diagram for the input sequence in (b). Show $P$, $X$, $A$, $B$, and $Z$. Assume that the input changes between clock pulses.

![Sequential Network Diagram]

13.5 (a) For the following sequential network, write the next-state equations for flip-flops $A$ and $B$.
(b) Using these equations, find the state table and draw the state graph.

![Sequential Network Diagram]
13.6 (a) Construct a state table and graph for the given network.
(b) Construct a timing chart for the network for an input sequence $X = 10011$. Indicate at what times $Z$ has the correct value and specify the correct output sequence. (Assume that $X$ changes midway between clock pulses.) Initially, $Q_1 = Q_2 = 0$.

![Diagram of a sequential network](image)

13.9 A sequential network has the form shown in Fig. 13–13 with

\[
D_1 = Q_2Q_3', \quad D_3 = Q_2' + X \\
D_2 = Q_3, \quad Z = XQ_2' + X'Q_2
\]

(a) Construct a state table and state graph for the network.

(b) Draw a timing diagram for the network showing $X$, clock, $Q_1$, $Q_2$, $Q_3$, and $Z$. Use the input sequence $X = 01011$ and assume that $X$ changes midway between clock pulses. Indicate any "false" outputs on the diagram.

(c) Compare the output sequence obtained from the timing diagram with that from the state graph.

(d) At what time with respect to the clock should the input be changed in order to eliminate the false output(s)?