Show your work! You will not receive full credit for the answer alone.

1. Design a counter that counts in the sequence: 101, 100, 011, 010, 001, 000, 101, ...
   Use clocked D flip-flops. Draw the circuit diagram. What will happen if your counter
   starts in an invalid state?

   \[\begin{array}{c|ccc|ccc}
   A & B & C & A+ & B+ & C+ & Da & Db & Dc \\
   \hline
   000 & \text{101} & \text{101} & \\
   001 & \text{000} & \text{000} & \\
   010 & \text{001} & \text{001} & \\
   011 & \text{010} & \text{010} & \\
   100 & \text{011} & \text{011} & \\
   101 & \text{100} & \text{100} & \\
   110 & \text{XXX} & \text{XXX} & \\
   111 & \text{XXX} & \text{XXX} & \\
   \end{array}\]

   Design Equations: \( Da = AC + A'B'C', Db = AC' + BC, Dc = C' \)
   If in state 110, NS is 011. If in state 111, NS is 110.

2. Repeat problem (1) using J-K flip-flops. You do not need to draw the circuit diagram.

   \[\begin{array}{c|ccc|cccc}
   A & B & C & A+ & B+ & C+ & Ja & Ka & Jb & Kb & Jc & Kc \\
   \hline
   000 & \text{101} & 1X & 0X & 1X & \\
   001 & \text{000} & 0X & 0X & X1 & \\
   010 & \text{001} & 0X & X1 & X1 & \\
   011 & \text{010} & 0X & X0 & X1 & \\
   100 & \text{011} & X1 & 1X & 1X & \\
   101 & \text{100} & X0 & 0X & X1 & \\
   110 & \text{XXX} & XX & XX & XX & \\
   111 & \text{XXX} & XX & XX & XX & \\
   \end{array}\]

   Design Equations: \( Ja = B'C', Ka = C', Jb = AC', Kb = C', Jc = 1, Kc = 1 \)
   If in state 110, NS is 001. If in state 111, NS is 111. It would be wise to redesign this
   state machine so state 111 leads to some valid state.
3. Design a counter that counts in the sequence: 000, 010, 001, 100, 011, 110, 000, ...
   Use clocked T flip-flops. Design your counter to go to state 000 from all invalid states.
   There is no need to draw a circuit diagram.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>A+ B+ C+</th>
<th>Ta</th>
<th>Tb</th>
<th>Tc</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>010</td>
<td>010</td>
<td></td>
<td></td>
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<tr>
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<td>1</td>
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<tr>
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<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>110</td>
<td>101</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>011</td>
<td>111</td>
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<td></td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>000</td>
<td>101</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>110</td>
<td>110</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>111</td>
<td>111</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Design Equations: \( Ta = A + C, \) \( Tb = C' + AB, \) \( Tc = C + A'B + AB' \)

4. Do problem 14.4 on page 380 of your text.

5. Do problem 14.7 on page 380 of your text.
   See solutions in your book for a state table. A 4-state state diagram is shown below.
6. (Optional, 2 points) Do problem 14.13 on page 381 of your text.

7. Design the state diagram for a Mealy-style clocked sequential network that investigates an input sequence $X$ and will produce an output $Z = 1$ for any input sequences ending in 1101 or 011. Example:

$$ X = 0 \ 0 \ 1 \ 1 \ 0 \ 1 \ 1 \ 0 \ 1 \ 0 \ 1 \ 1 \ 0 \ 1 \ 0 \\
Z = 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 1 \ 0 \ 1 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 $$

8. A 1-block is a consecutive sequence of 1s bounded on the left by 0 or by the left end of the sequence. Design a state table for a clocked sequential state machine that investigates an input sequence and will produce an output $Z = 1$ coincident with an input $X = 0$ that terminates a 1-block of even length (containing an even number of 1s). Example:

$$ X = 1 \ 1 \ 0 \ 1 \ 1 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 1 \ 1 \ 0 \ 1 \ 1 \ 1 \ 0 \ 1 \ 0 \\
Z = 0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0 $$

<table>
<thead>
<tr>
<th>PS</th>
<th>NS</th>
<th>X=0</th>
<th>X=1</th>
<th>X=0</th>
<th>X=1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S1</td>
<td>S1</td>
<td>S2</td>
<td>0</td>
<td>0</td>
<td>No 1s yet</td>
</tr>
<tr>
<td>S2</td>
<td>S1</td>
<td>S3</td>
<td>0</td>
<td>0</td>
<td>In a 1-block, odd # of '1's</td>
</tr>
<tr>
<td>S3</td>
<td>S1</td>
<td>S2</td>
<td>1</td>
<td>0</td>
<td>In a 1-block, even # of '1's</td>
</tr>
</tbody>
</table>
9. (6 points) Design a clocked Mealy sequential network that investigates an input sequence $X$ and that will produce an output $Z = 1$ if the total number of 1s received is even (consider zero 1s to be an even number of 1s) and the sequence 00 has occurred at least once. The total number of 1s received includes those received before and after 00. Example:

$X = 1\ 0\ 1\ 0\ 1\ 0\ 0\ 1\ 1\ 0\ 1$

$Z = 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1\ 0\ 0\ 1$

A minimum of six states is required. Design your network using NAND gates, NOR gates, and three J-K flip-flops. Assign 000 to the start state.

<table>
<thead>
<tr>
<th>PS</th>
<th>NS</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>X=0</td>
<td>X=1</td>
<td>X=0</td>
</tr>
<tr>
<td>S0</td>
<td>S1</td>
<td>S2</td>
</tr>
<tr>
<td>S1</td>
<td>S3</td>
<td>S2</td>
</tr>
<tr>
<td>S2</td>
<td>S4</td>
<td>S0</td>
</tr>
<tr>
<td>S3</td>
<td>S3</td>
<td>S5</td>
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<tr>
<td>S4</td>
<td>S5</td>
<td>S0</td>
</tr>
<tr>
<td>S5</td>
<td>S5</td>
<td>S3</td>
</tr>
</tbody>
</table>

$S0$: even # 1s, no 00
$S1$: even # 1s, and 0
$S2$: odd # 1s, no 00
$S3$: even # 1s and 00
$S4$: odd # 1s, and 0
$S5$: odd # 1s and 00

$J_a = BC'X' + BCX$, $K_a = X$, $J_b = CX + A'X + A'C$, $K_b = C' + X$.

$J_c = B'C'X'$, $K_c = A'B'X$, $Z = A'CX' + ACX$