- No additional registered I/O on memory (sync write / async read)
- Start with reset asserted; sim 50 cc after reset deasserted
- 2 PI, one (2-bit) PO

Initial memory using .COE file

- RSF
- OK
- PI
- RST
- CNTR
- (2:1)
- WE
- DOUT
- 4x2
- Z
- PO
- ISOLATED REG