Fig. 1. The structure of a DCVS circuit.

Fig. 3
(a) No diagram
(b) Load circuit diagram
(c) Additional load circuit diagram

Figure 7

Figure 8
TABLE I
TYPICAL LIST FORMAT FOR THE TABULAR METHOD

<table>
<thead>
<tr>
<th>Decimal representation of input vector</th>
<th>Input vector</th>
<th>Record 1</th>
<th>Record 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 4</td>
<td>0 0 1 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 6</td>
<td>0 1 1 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 7. The basic DCVS tree structure as it would develop from a tabular list.

TABLE III
THE 10-LIST OF A 3-BIT MAGNITUDE COMPARATOR

<table>
<thead>
<tr>
<th>Decimal representation of reduced input vector</th>
<th>Reduced Input vector</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( x_2 \ x_3 \ x_5 \ x_6 )</td>
</tr>
<tr>
<td>0</td>
<td>0 0 0 0</td>
</tr>
<tr>
<td>4</td>
<td>0 0 1 0</td>
</tr>
<tr>
<td>1</td>
<td>0 0 0 1</td>
</tr>
<tr>
<td>5</td>
<td>0 0 1 0</td>
</tr>
<tr>
<td>6</td>
<td>0 0 1 1</td>
</tr>
<tr>
<td>12</td>
<td>0 1 1 0</td>
</tr>
<tr>
<td>3</td>
<td>0 0 0 1</td>
</tr>
<tr>
<td>24</td>
<td>1 1 0 0</td>
</tr>
<tr>
<td>18</td>
<td>1 0 0 1</td>
</tr>
<tr>
<td>7</td>
<td>0 0 1 1</td>
</tr>
<tr>
<td>13</td>
<td>0 1 1 0</td>
</tr>
<tr>
<td>25</td>
<td>1 1 0 0</td>
</tr>
<tr>
<td>26</td>
<td>1 1 0 1</td>
</tr>
<tr>
<td>15</td>
<td>0 1 1 1</td>
</tr>
<tr>
<td>27</td>
<td>1 1 0 1</td>
</tr>
<tr>
<td>30</td>
<td>1 1 1 0</td>
</tr>
</tbody>
</table>

Fig. 8. The shared DCVS tree circuit corresponding to the 10-list of Table IV.
TABLE V
THE 1-LIST AND ITS MINIMAL SUM FOR THE MAGNITUDE COMPARATOR

<table>
<thead>
<tr>
<th>Decimal representation of input vector</th>
<th>Input vector $x_1 x_2 x_3 x_4 x_5 x_6$</th>
<th>$p_i$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0 0 0 0 1 0</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>0 0 1 0 0 0</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>0 0 1 0 0 1</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>0 0 1 0 1 0</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>1 0 1 0 0 0</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>1 0 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>0 0 1 0 1 1</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>0 0 1 1 1 0</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>1 0 1 0 0 1</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>1 0 1 0 1 0</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>1 0 1 0 1 1</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>1 0 1 1 1 0</td>
<td></td>
</tr>
</tbody>
</table>

minimal sum $= x_2 x_3 x_5 \overline{x_6} + x_2 x_4 x_5 \overline{x_6} + x_2 x_3 x_4 \overline{x_6}$

$\begin{align*}
\text{Fig. 9.} & \quad \text{The complete DCVS tree for the 3-bit magnitude comparator.}
\end{align*}$