

Introduction to VHDL

Coding for Synthesis

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VHDL

- ❑ VHSIC Hardware Description Language
- ❑ NOT a programming language!
- ❑ Hierarchical Modeling
- ❑ Hardware Abstraction
- ❑ Synchronous and Asynchronous Logic
- ❑ Combinational and Sequential Logic

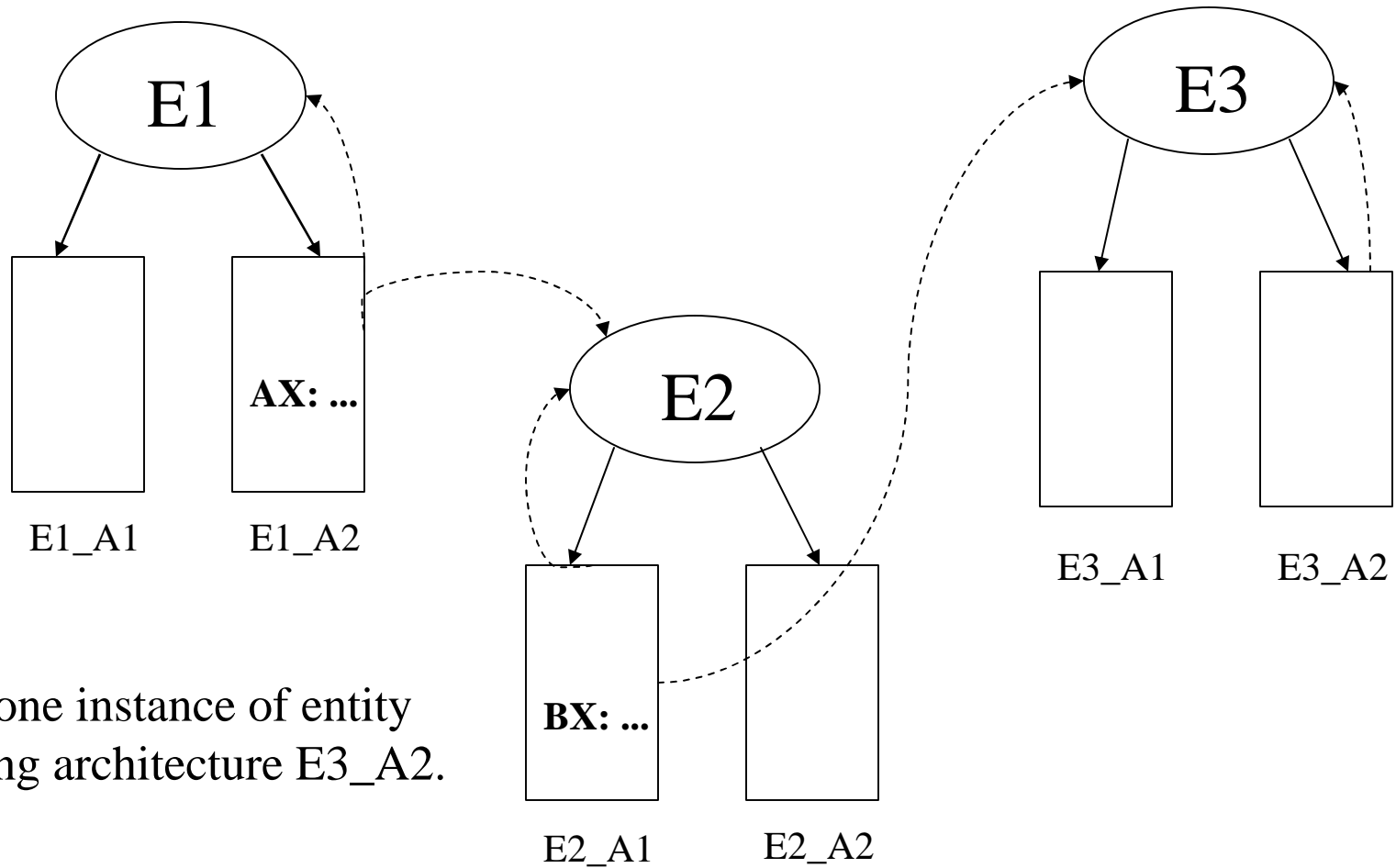
Hierarchy

- ❑ A design consists of components
- ❑ Each component has an entity and one or more architectures
- ❑ The entity describes the I/O interface
- ❑ The architecture models the function of the component
- ❑ When a component is used in a design (instantiated), an entity-architecture pair is specified.

Design Flow

- ❑ Produce the VHDL Model
- ❑ Compile the VHDL
- ❑ Simulate the compiled VHDL to verify function
- ❑ Synthesize/Optimize to a technology
- ❑ Simulate again to verify timing

Configuration



BX is one instance of entity E3 using architecture E3_A2.

Entity Port Types

- ❑ In: value read within entity model
- ❑ Out: value updated within entity model; cannot be read.
- ❑ Inout: bidirectional port; can be read and updated.
- ❑ Buffer: can be read and updated within the entity model.
Can only have one source.

Avoid using "Buffer"!!!! Instead, use an internal signal and a concurrent assignment. e.g., `my_out <= my_out_internal;`

Modeling Styles

- ❑ Structural: Used to describe the interconnection of primitive and user-defined components.
- ❑ Dataflow: Provides logical and arithmetic operators.
- ❑ Behavioral: Allows modeling using if-then, case statements, etc.

Architecture

❑ Interconnected components (structural)

❑ Concurrent Statements (dataflow)

Executed in “parallel”. Order independent.

❑ Sequential Statements (behavioral)

Executed sequentially inside a process. Order dependent.

Identifiers

- ❑ (A-Z), (a-z), (0-9), underscore.
- ❑ First character is a letter, last not an underscore.
- ❑ Two consecutive hyphens starts a comment.
- ❑ Case insensitive. (except for type values, e.g., 'Z')

Data Objects

- ❑ Constants
- ❑ Variables
- ❑ Signals: Maintain a history. Permits modeling of delays, detection of edges.

Types

- ❑ Enumerated Types
- ❑ Single bit and bit-vector signals
- ❑ Symbolic States

Operators

- ❑ Logical: and, or, nand, nor, xor, not, xnor (VHDL-93)
- ❑ Relational: =, /=, <, <=, >, >=
- ❑ Adding: +, -
- ❑ Concatenation: &
- ❑ Multiplying: *, /, mod, rem
- ❑ Misc: abs, **

Architecture Revisited

```
architecture [name] of [entity name] is
    [declarations]
begin
    concurrent statements;
    (e.g., signal assignments, process statements,
     component instantiations)
end [name];
```

Concurrent Signal Assignment

```
sig4 <= (sig1 AND sig2) OR (sig3 AND (not sig2));
```

Useful for modeling small combinational logic circuits.

With - Select

with (expression) select

Sig <= (expression) WHEN (choice),
(expression) WHEN (choice),
(expression) WHEN others;

- ❑ The "choices" must be mutually exclusive.
- ❑ "Choices" are possible values of the expression.
- ❑ "when others" covers any possibilities not listed and avoids latches.

When - Else

```
Sig <= (expression) WHEN (condition) ELSE  
      (expression) WHEN (condition) ELSE  
      (expression);
```

Important to finish with ELSE, rather than WHEN, to eliminate the potential for implied latches.

"Conditions" are Boolean (e.g.. X = '0', true or false)

Enforces priority, which may lead to more logic than with-select if the conditions are mutually exclusive.

Process Statement

```
[process label:] process [(sensitivity list)]  
    [process declarations]  
begin  
    sequential statements;  
    (signal assignments, if statement, case statement)  
end process [process label];
```

- ❑ If modeling combinational logic then all inputs must be in the sensitivity list.
- ❑ If modeling sequential logic then usually only the clock is in the sensitivity list.

If Statement

```
if (boolean expression) then
    sequential statements;
elsif (boolean expression) then
    sequential statements;
else
    sequential statements;
end if;
```

Note the weird spelling of elsif!

Equivalent to the concurrent conditional
signal assignment, when-else

Case Statement

```
case (expression) is
  when (choices) => sequential statements;
  [...]
  when others => sequential statements;
end case;
```

Equivalent to the concurrent selected
signal assignment, with-select

Tips from the Master

- ❑ Think hardware. If you don't know what it will synthesize to, don't write it.
- ❑ Specify signal values under all occurrences (end with “else” or “when others”). Specify default at the start of a process.
- ❑ Separate out next state logic and output logic (or state flip-flops and combinational logic).
- ❑ Partition, partition, partition!

```

entity FULL_ADDER is
    port (A, B, CIN: in std_logic; SUM, COUT: out std_logic);
end FULL_ADDER;
architecture FA_MIXED of FULL_ADDER is
    component XOR2
        port (P1, P2: in std_logic; PZ: out std_logic);
    end component;
    signal S1: BIT;
begin
    X1: XOR2 port map (A, B, S1);           - structural
    process (A, B, CIN)                     - behavioral
        variable T1, T2, T3: std_logic;
    begin
        T1 := A and B;                       Variables used to
        T2 := B and CIN;                     model internal wires
        T3 := A and CIN;
        COUT <= T1 or T2 or T3;
    end process;
    SUM <= S1 xor CIN;                       - dataflow
end FA_MIXED;

```

Figure 2.7 A 1-bit full-adder.

