Continuous-Time Sigma Delta Modulators for High Resolution Wideband Analog to Digital Conversion

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Abstract: Although sigma delta analog to digital data converters (ADCs) have been mostly implemented using discrete-time circuits, continuous-time implementation of such ADCs offers significant advantages in realizing high speed, high resolution and low power ADCs.

A new continuous-time (CT), discrete-time (DT) cascaded sigma delta modulator (SDM) will be introduced. The combination of a CT first stage and a DT second stage can be used to realize a high speed, high resolution analog-to-digital converter (ADC). Power consumption of CT first stage is lowered by optimizing the gain coefficients of CT integrator in a feedforward topology. Moreover, correlated double sampling (CDS) was used in second stage integrators to further reduce power consumption. Proposed new SDM is simulated in 0.18um CMOS technology and achieves 84dB dynamic range for a 10MHz signal bandwidth. Total analog power dissipation measured was 44mW.

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